# A Filter Synthesis Technique Applied to the Design of Multistage Broadband Microwave Amplifiers

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*Abstract*— **A synthesis method for designing multistage broadband amplifiers based upon well known filter synthesis techniques is presented. Common low-pass approximations are used to synthesize the amplifier circuit. A proof of concept Butterworth low-pass two-stage amplifier was designed, simulated and measured, and achieved a flat gain performance of 1-4GHz with a gain of $15 \pm 1dB$ as predicted. A comparison is made with the distributed amplifier (DA) and the cascaded single stage distributed amplifier (CSSDA). Theoretically a larger gain bandwidth product is achieved using the synthesis technique.**

## I. Introduction

The distributed amplifier (DA) has been firmly established for two decades in the design of amplifiers spanning multi-octave bandwidths [1], [2]. The advantages of this type of amplifier are flat gain, flat group delay, low noise figure and low voltage standing wave ratio performance over broad bandwidths. The key applications for this type of amplifier are warfare electronics and digital optical communications.

The main disadvantage of the DA is the high number of devices per unit gain. The cascaded single-stage distributed amplifier (CSSDA) matches the bandwidth of the DA, but by cascading single stages increases the gain significantly [3], [4]. This technique relies upon computer optimization techniques to meet the final design specification, but this non-scientific method is costly in terms of design hours.

The technique proposed herein allows the synthesis of multistage amplifiers to within a close tolerance of the initial design specifications without reliance on computer optimization. The amplifier response can be fully specified using Butterworth, Chebyshev, Bessel or other all-pole approximations to the ideal low-pass response.

## II. Synthesis procedure

The schematic of a simple equivalent circuit model (ECM) for a GaAs MESFET is shown in Fig. 1. The transfer function of this circuit is given by:

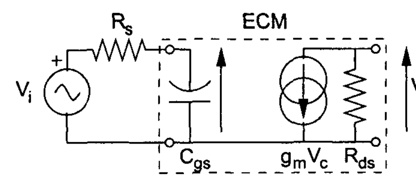


Fig. 1. Simple unilateral equivalent circuit model for a GaAs MESFET.

$$\frac{V_o(p)}{V_i(p)} = \frac{-g_m R_{ds}}{1 + pC_{gs}R_s} \tag{1}$$

and the 3dB cutoff frequency for the MESFET is therefore:

$$\omega_{3dB} = \frac{1}{C_{gs}R_s} \tag{2}$$

It is well known that the bandwidth of the amplifier can be extended and the gain flattened by adding a series inductor to the gate of the MESFET.

The transfer function now becomes second order with two complex conjugate transmission poles, i.e.

$$\frac{V_o(p)}{V_i(p)} = \frac{-g_m R_{ds}}{1 + pC_{gs}R_s + p^2 L_g C_{gs}} \tag{3}$$

The transmission pole locations, see Fig. 2, may be solved, where $p_{1,2} = -\alpha \pm j\beta$.

$$\alpha = \frac{R_s}{2L_g} \tag{4}$$

$$\beta = \sqrt{\frac{1}{L_g C_{gs}} - \left(\frac{R_s}{2L_g}\right)^2} \tag{5}$$

$$\omega_o = \frac{1}{\sqrt{L_g C_{gs}}} \tag{6}$$

A Butterworth, Chebyshev or other all-pole approximation to the ideal low-pass response can be synthesised from this simple RLC circuit. There are well





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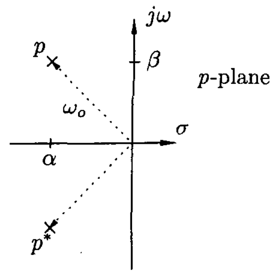


Fig. 2. Pole zero plot in the complex frequency plane for a second order tranfer function.

| Order $n$ | Dimension | Butterworth | Chebyshev (1dB Ripple) |
|---|---|---|---|
| 2 | $\alpha$ | 0.707 | 0.549 |
| | $\omega_o^2$ | 1 | 1.103 |
| 4 | $\alpha_1$ | 0.383 | 0.984 |
| | $\omega_{o1}^2$ | 1 | 0.987 |
| | $\alpha_2$ | 0.924 | 0.407 |
| | $\omega_{o2}^2$ | 1 | 0.279 |

TABLE I
POLE LOCATIONS FOR BUTTERWORTH AND CHEBYSHEV LOW-PASS APPROXIMATIONS.

known general methods of synthesizing singly terminated networks to produce a given transfer function [5]. The following simple technique considers second order tranfer functions only.

The pole positions of Butterworth and Chebyshev low-pass approximations are given in Table I. Solving (4) and (6) for $L_g$ and $C_{gs}$ respectively yields the prototype circuit element values for the chosen approximation.

$$L_g = \frac{R_s}{2\alpha} \tag{7}$$

$$C_{gs} = \frac{1}{\omega_o^2 L_g} = \frac{2\alpha}{\omega_o^2 R_s} \tag{8}$$

Once the prototype circuit is known, it is scaled in frequency to suit the MESFET used. The cut off frequency is given by:

$$\omega_{3dB} = \frac{2\alpha}{\omega_o^2 R_s C'_{gs}} \tag{9}$$

where $C'_{gs}$ is the gate source capacitance of the MESFET. Comparing (9) with (2) demonstrates that $\omega_{3dB}$ is increased by a factor $2\alpha/\omega_o^2$. The schematic for an amplifier with $n$-stages is presented in Fig. 3 and the transfer function is given by:

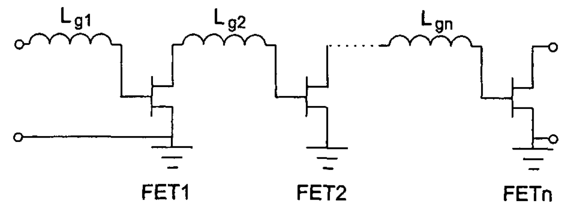


Fig. 3. Schematic of a $n$-stage amplifier with matching inductors $L_{gi}$.

$$S_{21}(p) = \frac{2(-1)^n \prod_{i=1}^{n} g_{mi}}{(G_{dsn} + Y_s)(\mathcal{F}_1(p)) \prod_{i=2}^{n} (\mathcal{F}_i(p))} \tag{10}$$

where

$$\mathcal{F}_1(p) = (1 + pC_{gs1} + p^2 C_{gs1} L_{g1}) \tag{11}$$

$$\mathcal{F}_i(p) = (G_{ds(i-1)} + pC_{gsi} + p^2 C_{gs} i L_{gi} G_{ds(i-1)}) \tag{12}$$

The denominator of the transfer function in (10) contains $n$ quadratic factors; each quadratic factor is contributed by the corresponding $i^{th}$ FET and matching inductor $L_{gi}$. Each stage therefore contributes a pair of complex conjugate poles, whose position is determined by the value of the circuit elements $C_{gs}$, $L_g$, $R_{ds}$ and the source impedance $R_{si}$. For $C_{gsi} = C_{gs1}$

$$R_{inti} = \frac{\alpha_i \omega_{o1}^2}{\alpha_1 \omega_{oi}^2} R_s \tag{13}$$

Where $R_{inti}$ is the source resistance seen by the $i^{th}$ stage looking back towards stage $(i-1)$.

It is therefore possible to synthesize such an amplifier topology to exhibit a prescribed transfer function. A $n$-stage amplifier will contribute $n$ pairs of complex conjugate transmission poles, as each stage will contribute one isolated pair. It is possible to control the amplifier response through the choice of poles that each stage contributes. For example, a two stage design has two possible realisations. The first stage may contribute the poles closest to the $j\omega$-axis for maximum gain, or the poles closest to the $\sigma$-axis for maximum bandwidth. In general for $n$-stages there are $(n-1)n$ permutations. The order of the approximation required is 2n, so for two stages a fourth order all-pole approximation is realisable.

## III. Comparison with cascaded single stage distributed amplifier

The DC performance of the DA, CSSDA and synthesis method is now compared. The equations describing DC forward available gain, $G_{av}$, for each using ideal lossless $n$-stage devices are given in Table II. It can

| DA [6] | CSSDA [4] | Synthesis |
|---|---|---|
| $\frac{n^2 g_m^2 Z_L Z_S}{4}$ | $\frac{g_m^{2n} Z_{int}^{2(n-1)} Z_L Z_S}{4}$ | $4 g_m^{2n} Z_L Z_S \prod_{i=1}^{n-1}(R_{inti}^2)$ |

TABLE II
COMPARISON OF FORWARD AVAILABLE GAIN, $G_{av}$ FOR THREE AMPLIFIER TYPES.

be seen from Table II that in order for the CSSDA to achieve higher gains than the DA, the following inequality relationship must be satisfied [4]:

$$Z_{int} \geq \frac{\sqrt[n-1]{n}}{g_m} \tag{14}$$

It has been demonstrated that the CSSDA provides more gain per device than the DA [3]. The synthesis method realises 12dB more gain than the CSSDA for identical interstage impedances. This is due to the input and output matching of the CSSDA. Input and output match can also be achieved in the synthesis design, at a cost of 12 dB gain, but this is beyond the scope of this paper. Accounting for the loss in gain due to matching, we now compare the gain bandwidth products (GBW) for the two amplifiers. The radian cut-off frequency of the CSSDA is given by [7]

$$\omega_c = \frac{2}{C_{gs} R_s} \tag{15}$$

and therefore the GBW product for the CSSDA is:

$$GBW_{CSSDA} = \frac{g_m^{2n} Z_{int}^{2(n-1)} Z_L Z_S}{2 C_{gs} R_s} \tag{16}$$

and for the synthesis method from (9) and Table II, the GBW product is:

$$GBW_{synthesis} = \frac{8 \alpha_1 g_m^{2n} Z_L Z_S \prod_{i=1}^{n-1}(R_{inti}^2)}{\omega_o^2 C_{gs} R_s} \tag{17}$$

Comparing (16), (17) and allowing for 12 dB more gain from the unmatched synthesised amplifier demonstrates that for the CSSDA to have a larger GBW product than the synthesis amplifier, the following must hold:

$$Z_{int} \geq \sqrt[2(n-1)]{\frac{\alpha_1}{\omega_{o1}^2} \prod_{i=1}^{n-1}(R_{inti}^2)} \tag{18}$$

Table III indicates the GBW advantage of the synthesis amplifier when compared to the CSSDA and therefore the CDA. The results are for Butterworth and Chebyshev amplifiers designed for maximum GBW product. In practice Chebyshev amplifiers above two-stages cannot be realised due to the large values of $R_{ds}$ required ($\geq 400\Omega$).

| | $Z_{int}$ | |
|---|---|---|
| Stages | Butterworth | Chebyshev |
| 2 | $\geq 74.7\,\Omega$ | $\geq 160.29\,\Omega$ |
| 3 | $\geq 113\,\Omega$ | $\geq 300.2\,\Omega$ |
| 4 | $\geq 149.9\,\Omega$ | $\geq 432\,\Omega$ |

TABLE III
MINIMUM $Z_{int}$ REQUIRED FOR CSSDA TO MATCH GBW PRODUCT OF SYNTHESIS METHOD.

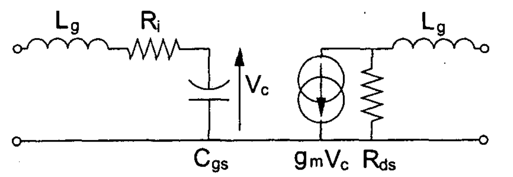


Fig. 4. Unilateral ECM used in the synthesis of a two-stage amplifier.

## IV. Design example

A NE71083 GaAs MESFET was used as the active device in a Butterworth two-stage amplifier design. The first stage in the design is to characterize the MESFET using a very simple ECM. This can be determined from manufacturers or measured $S$-parameters of the device using well known techniques [8]. The ECM used is shown in Fig. 4 and the circuit element values are given in Table IV.

The prototype circuit is then determined using (7),(8),(13) and Table I; $R_{s1} = R_s + R_i$, $R_{si} = R_{inti} + R_i$: $f_{3dB} = 4.27\ GHz$ (9): and the circuit elements are scaled in frequency and impedance. Table V tabulates the prototype and scaled circuit element values. The DC gain is given by (10) for the two-stage amplifier using the NE71083, $|S_{21}(0)|_{dB} = 26dB$. In practice parasitic elements and feedback will degrade the optimum performance.

## V. Simulation results

The simple unilateral ECM, shown in Fig. 4, was used as the active device in an ideal simulation along with lumped matching componenets. This was then compared to the same design using the NE71083 manufacturer's linear $s$-parameters and non-ideal matching components.

The synthesis technique in the ideal case produces a fourth order Butterworth response with a gain of 26dB as predicted and a $BW_{3dB}$ of 4.27 GHz. The response is degraded from the ideal when linear $s$-parameters, non-ideal circuit elements and FET bias are included in the simulation, see Fig. 5. This is to be expected

| Circuit element | Value |
|---|---|
| $L_g$ | 0.4 nH |
| $R_i$ | 7 Ω |
| $C_{gs}$ | 0.5 pF |
| $g_m$ | 0.043 S |
| $R_{ds}$ | 250 Ω |
| $L_d$ | 0.3 nH |

TABLE IV

CIRCUIT ELEMENT VALUES FOR THE NE71083 ECM. $V_{ds} = 3V, I_{ds} = 10mA$

| Element | Prototype | Scaled |
|---|---|---|
| $L_{g1}$ | 1.489 H | 2.77 nH |
| $C_{gs1}$ | 0.671 F | 0.5 pF |
| $L_{g2}$ | 1.489 H | 2.77 nH |
| $C_{gs2}$ | 0.671 F | 0.5 pF |
| $R_{ds1}$ | 2.612 Ω | 130.61 Ω |

TABLE V

PROTOTYPE AND SCALED CIRCUIT ELEMENT VALUES FOR A BUTTERWORTH TWO-STAGE AMPLIFIER.

as parasitic and feedback elements were not accounted for in the synthesis procedure, and neither were the practical realisation of matching inductors and shunt resistance. However the response exhibits a gain of $18 \pm 1dB$ over a $\text{BW}_{3dB}$ of 1 to 4.27 GHz.

## VI. MEASUREMENT RESULTS

The amplifier gain was measured as $14 \pm 1dB$ over a $\text{BW}_{3dB}$ of 1 to 4.1 GHz (see Fig. 5). The discrepancy between simulated and measured results is due to the FET characterisation method. The MESFET is currently being characterised using a test fixture that reproduces the circuit environment found in the amplifier realisation; it is believed closer predicted and measured performance will follow. No tuning was necessary to achieve this response.Gain $\geq 20dB$ is measured at low frequencies; this is explained by DC blocking capacitors increasing $R_{int}$. An alternative bias topology will allow low frequency operation.

## VII. CONCLUSION

The theoretical development of a simple filter synthesis technique applied to the design of multistage broadband amplifiers has been presented. This method has been proven correct through simulated and measured results of a proof-of-concept Butterworth two-stage amplifier. The technique can, in theory, be extended to any bandwidth and gain required by the designer, provided suitable MESFETs are available. The technique is particularly suited to MMIC amplifier design where associated parasitic components are minimal, and large bandwidths are theoretically achievable. Any all-pole transfer function may be realised using this technique, making it particulary useful in realising amplifiers for digital optical communications where flat group delay is desired. Input and output matching may also be improved by utilising all-pass networks at the input and output, although 6dB loss will occur for each.

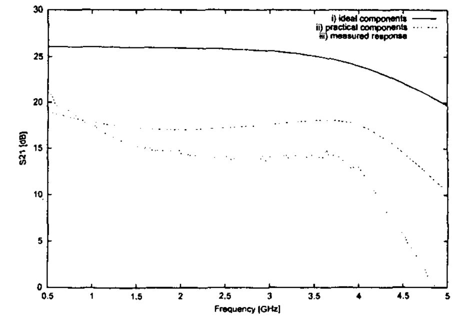


Fig. 5. Two-stage Butterworth amplifier using the NE71083 MESFET. Simulated responses using i) ideal components, ii) practical components vs. iii) measured response.

## ACKNOWLEDGMENT

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